Technical Specification of the Number Smasher-860 FIFO Interface

V 1.0

INTRODUCTION

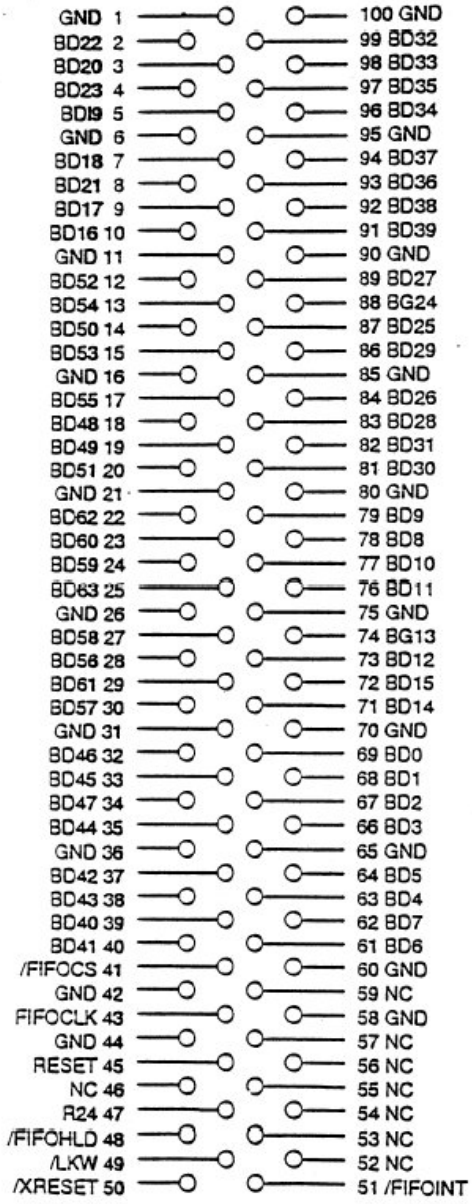
This document describes the 100-pin FIFO interface connector on Microway's Number Smasher-860, and some details on designing PC adapter boards that use this interface. The FIFO interface is used to connect Microway's FIFO I/O boards (both ISA and EISA versions) to the Number Smasher-860. This specification is provided to assist hardware designers who are interested in developing custom peripherals to the Number Smasher-860 using the interface. While this description is considered accurate, no guarantee is made by Microway. This specification and the hardware it describes are subject to change without notice.

SIGNAL DESCRIPTIONS

/XRESET	(Input)	Active low board reset input: has 3.3K pullup. Asserting /XRESET will cause RESET, below, to assert.
/FIFOHLD	(Input)	Active low "wait" signal: inserts wait states during FIFO data transfer cycles.
/FIFOINT	(Input)	Active low interrupt request to the i860. OR'ed with all other i860 hardware interrupt signals to drive i860 INT/CS8 pin. Has 3.3K pullup.
RESET	(Output)	Active high CPU reset. This signal drives the i860 RESET pin. The i860 can be reset from either the on-board link interface or the FIFO /XRESET signal.
FIFOCLK	(Output)	Reference clock, same frequency as i860 (33 MHz or 40 MHz).
/FIFOCS	(Output)	Active low. On-board PALS drive /FIFOCS low during FIFO read or write transfers. /FIFOCS's active width can be increased by asserting /FIFOHLD.
/LKW	(Output)	Active low. With /FIFOCS, indicates a FIFO write cycle.
A24	(Output)	This is a direct connection to the i860 A24 address line. A24 is used to select whether the FIFO data port (A24=1) or control port (A24=0) is being accessed.
BD0-BD63	I/O	This is the buffered i860 data bus. 74F245 transceivers are used on the Number Smasher-860 board to drive this data bus. The i860 is directly connected on the opposite side of the transceivers.
NC		No Connection on the current Number Smasher-860. RESERVED for future definition by Microway.
GND		Tied to the PCB ground plane (0V).

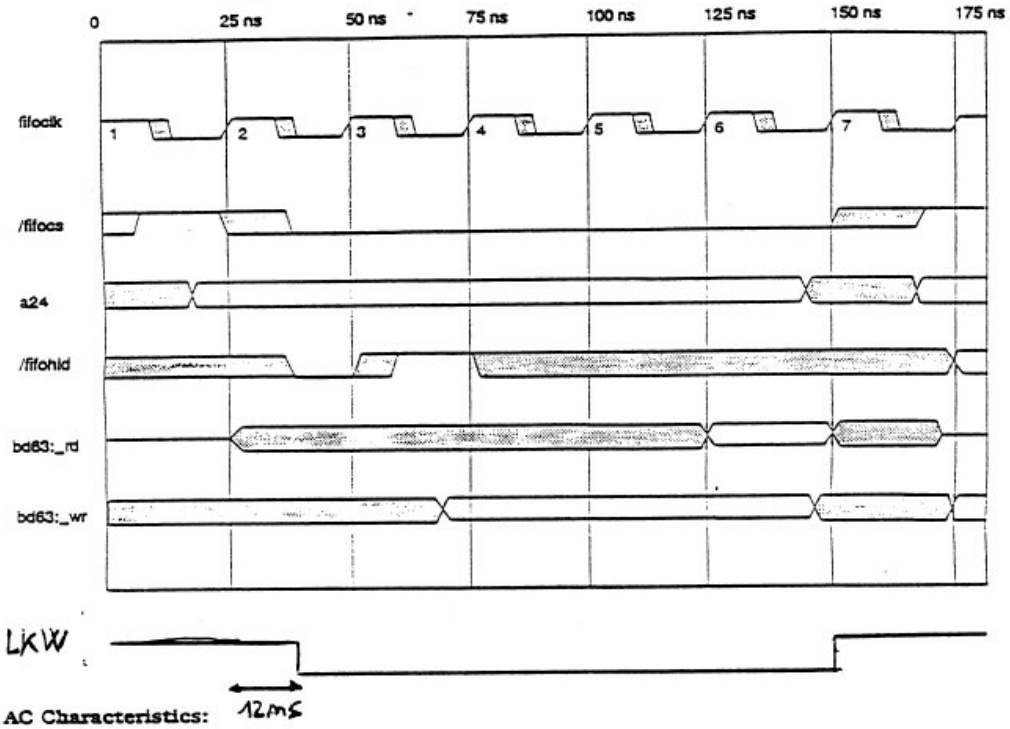
CONNECTOR PINOUT

The 100-pin connector's signal assignment is shown below. This is a view of the connector's hole pattern on the component side of the Number Smasher-860 printed circuit board (PCB).



..C. SPECIFICATION & TIMING DIAGRAM

Timing Diagram



AC Characteristics:

All figures below are in nanoseconds.

40MHz clock speed is assumed. Designing to these specs will also ensure compatibility with 33MHz product.

Description	Edge	Time	Notes
All cycles:			
FIFOCS active delay:	2	12 ns Max	(Notes 1,2)
FIFOCS inactive delay:	7	19 ns Max	
FIFOHLD setup:	3.4	12 ns Max	(Notes 1,2)
FIFOHLD hold:	3.4	2 ns Min	
LKW valid delay:	2	12 ns Max	
LKW invalid delay:	7	1 ns Min	
A24 valid delay:	1	18 ns Max	
A24 invalid delay:	7	-4.5 ns Min	

Description	Edge	Time	Notes
Read cycles:			
DATA setup:	7	24 ns Min	
DATA hold:	7	0 ns Min	
FIFOCS to DATA low impedance:	n/a	0 ns Min	(Note 3)
DATA high impedance delay:	7	21 ns Max	
Write cycles:			
DATA valid delay:	3	21 ns Max	
DATA invalid delay:	7	-3 ns Min	

Notes:

1. If FIFOHLD is tied inactive, the cycle length is five CPU clocks, and FIFOCS is active for four clocks. Add one CPU clock for each P2 CLK rising edge on which FIFOCS and FIFOHLD are both active. The diagram shows one such extra clock.

2. FIFOCS valid delay (max) and FIFOHLD setup (min) are such that it is not realistically possible to drive FIFOHLD active in response to FIFOCS active. Therefore, if cycles longer than 5 CPU clocks are desired, the idle state of FIFOHLD (between cycles) should be active. In this case, the fastest cycle will be 6 CPU clocks.

3. FIFOCS to data low impedance delay is a signal-to-signal spec. All others are clock-to-signal or signal-to-clock. If the data bus driver is enabled in response to FIFOCS, or some clock edge thereafter, this spec will automatically be met.

4. All valid delays, setup & hold times are relative to the rising edge of the clock on the P2 connector. This is not the same clock as the CPU clock, nor is it the same as the clock driving the PALs on the 860 board. Worst-case skews have already been incorporated in these figures.

INTERCONNECT BOARD

The Interconnect Board shown below is used to connect the Number Smasher-860 and a FIFO I/O adapter. This board and all of the connectors shown are available from Microway. Contact Microway for pricing.