Revision		
Sep 19 1991	Art Sobel	First draft
Oct 28 1991	Art Sobel	FORKED - Reduction of system to X version and simplifierd
Nov 25 1991	Art Sobel	Breakpoint put on external Logic analyser board. Released to layout
Feb 10 1992	Art Sobel	Corrections made to block diagram etc.
April 9 1992	Art Sobel	Converted to RC-600
June 8 1992	Art Sobel	Converted to VY86PID
March 16 1995	Art Sobel	Start PID III Includes ethernet
Aug 8 1995	Art Sobel	PID III rev A
Feb 15 1996	Art Sobel	PID III rev B Changed serial port to 16C552, Partner ET support

VY86PID III
Jump Start Board

Processor Independent Development Board for

ARM610/710/810 CPUs

With Cache and MMU

Table of Contenets

1.0 INTRODUCTION

The VY86PID is a host processor independant development board designed to aid ARM developers to generate software and hardware applications for the ARM product line. the VY86PID encorporates an Advanced RISC Machine CPU with Cache and MMU, fast PGAs (Programable Gate Arrays), and inexpensive, high integration peripheral components. Program development is aided by encorporation of a dedicated logic analyzer connector. the logic analyzer can be used monitor the ARM instructions for rapid software debug and can be triggered by a software breakpoint, or o ther event on the board by customer added logic. With CPU modules that support the ICE Breaker, embedded hardware breakpoint and the BlackICE serial ICE can also be used.
\pThe VY86PID i s made for the many users will be generating designs and writing code for fast I/O control, video games and graphics, disk caching, page printer controllers, OCR, etc.

the ARM RISC concept provides more computing power per silicon area and is a cost effective way to higher performance in many embedded applications. the VY86PID series development boards are expected to aid software and hardware developers in generating their own applications and hardware. the initial operating environment is to be monitor based with an expected progression to a real time multitasking operating system.

1.1 FEATURES

PROCESSOR	ARM610/710/810 Processors with Cache and Memory Management in CPU Module
FLOATING POINT	VY86C1010 - FPA10 Floating Point Co-Processor with ARM700 CPU Modules
ROM	4x 27C256 to 4x 27C080 (128K to 4 MB) EPROM
MAIN MEMORY	1,4,16 MByte memory with 256K, 1M, 4Mx8 bit DRAM SIMMs
OPERATING SYSTEMs	ROM Monitor (initially) and Remote Debugger
COMUNICATIONS	RS-232 serial port, Centronics printer port, 10BaseT Ethernet
EXPANSION	PC "AT" Style connector 32 bit data, 4Mbyte Address, Dual row connector All major components are on Main Board.

2.0 Hardware Description

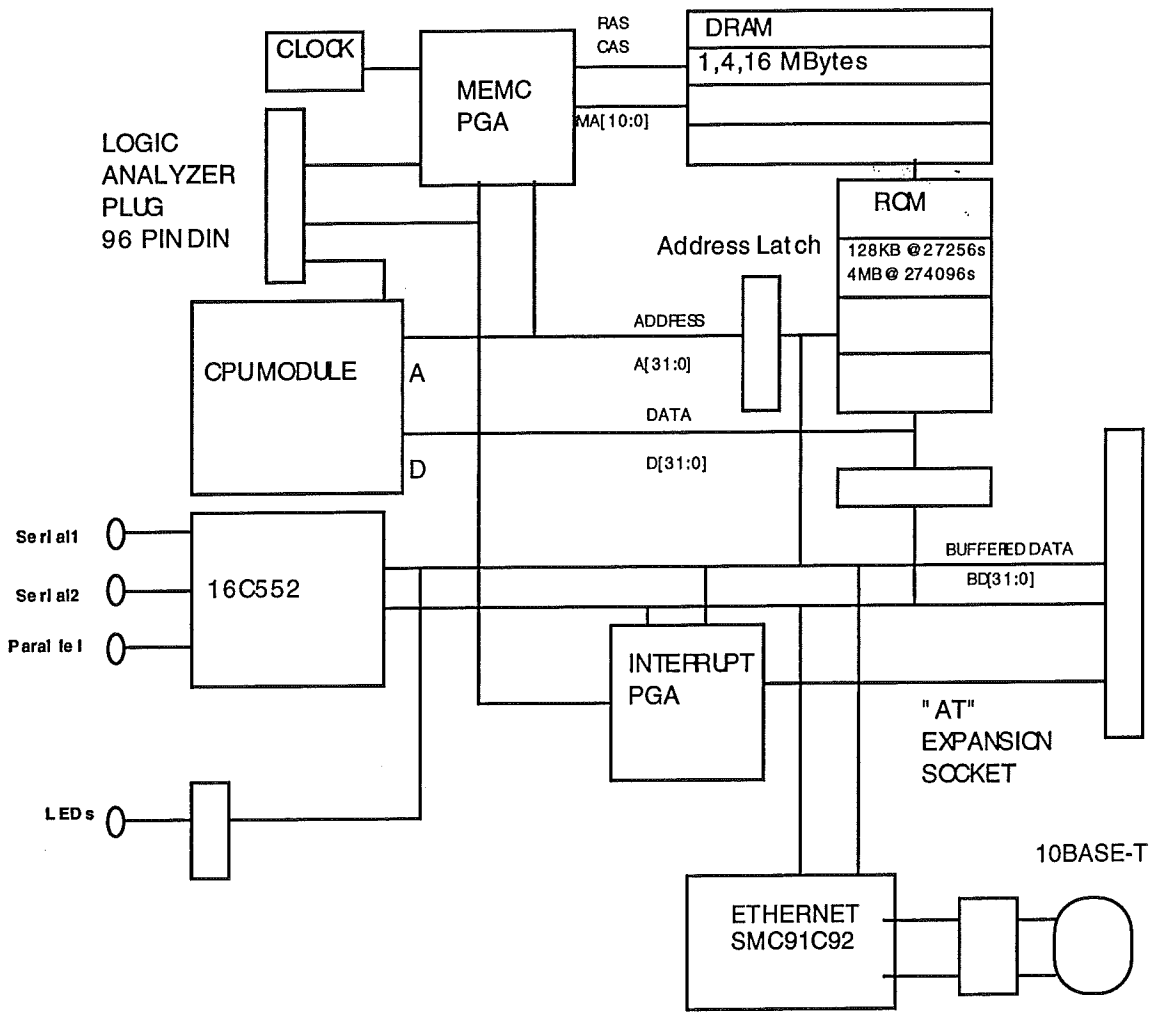
2.1 Board:

Th VY86PID is built on a PCB of 8 inches by 8 inches. the board is shipped with 1 Mbyte of DRAM and 256KByte of EPROM on which is written the ARM remote debugger Monitor (DEMON or ANGEL), startup and self check code and a floating point emulator.

2.2 Connectors:

Serial port to 38.4Kbaud	(DB-9, M ale, PC pinout)
Centronics Printer port	(DB-25, Female , PC pinout)
10 Base-T E thernet	8 Pin RJ-45 Telco
"AT" style Expansion	62 pin and 36 pin dual row edge conncetors
Logic Analyzer Port	96 pin tripple row female DIN
Power	4 Pin male Disk Drive, Molex

PID3 DEVELOPMENT BOARD



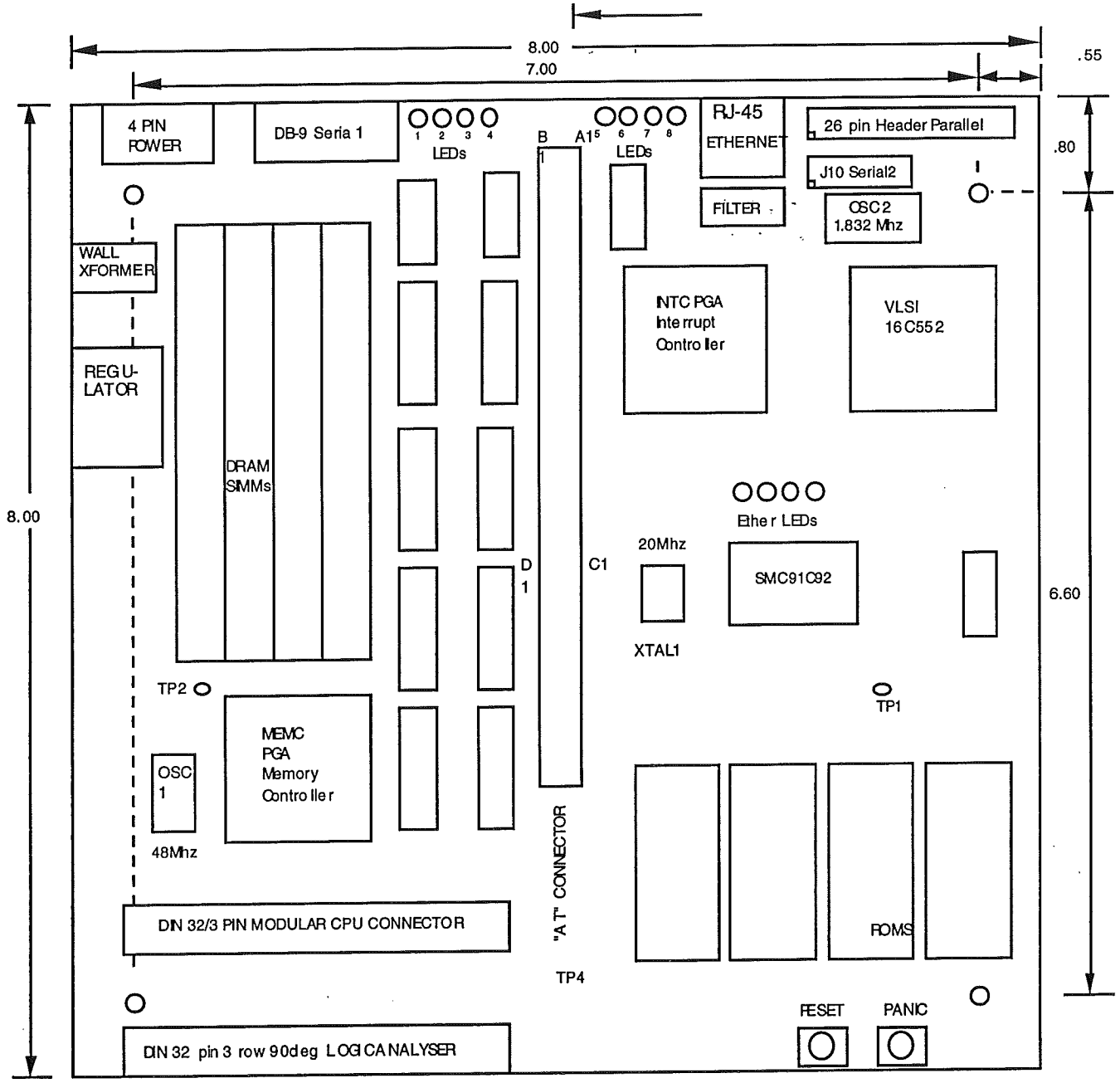


Figure 2 - VY86XPID3 RevB Board Layout

2.3 Main Component list:

Modular Processor	ARM610/7610/810	VLSI/GPS/Digital
QL8x12	Memory Controller PGA	VLSI/ QuickLogic
QL8x12	Interrupt Controller PGA	VLSI/ QuickLogic
VL16C552	Dual Serial Port with FIFO Bi-directional Parrallel Port	VLSI
SMC91C92	E thernet Controller	SMC
30Pin SIMMs	256Kx8Bit by 4 Bytes = 1 MByte 1Mx 8 Bit by 4 Bytes = 4 MByte 4Mx 8 Bit by 4 Bytes = 16 MByte	
28/32 Pin EPROM	27C256 = 128K Bytes 27C040 = 2 Mbytes	

2.3.1 Expansion Boards

Option cards are 13.12x3.9 inches with external I/O side mounted as in PC or AT.

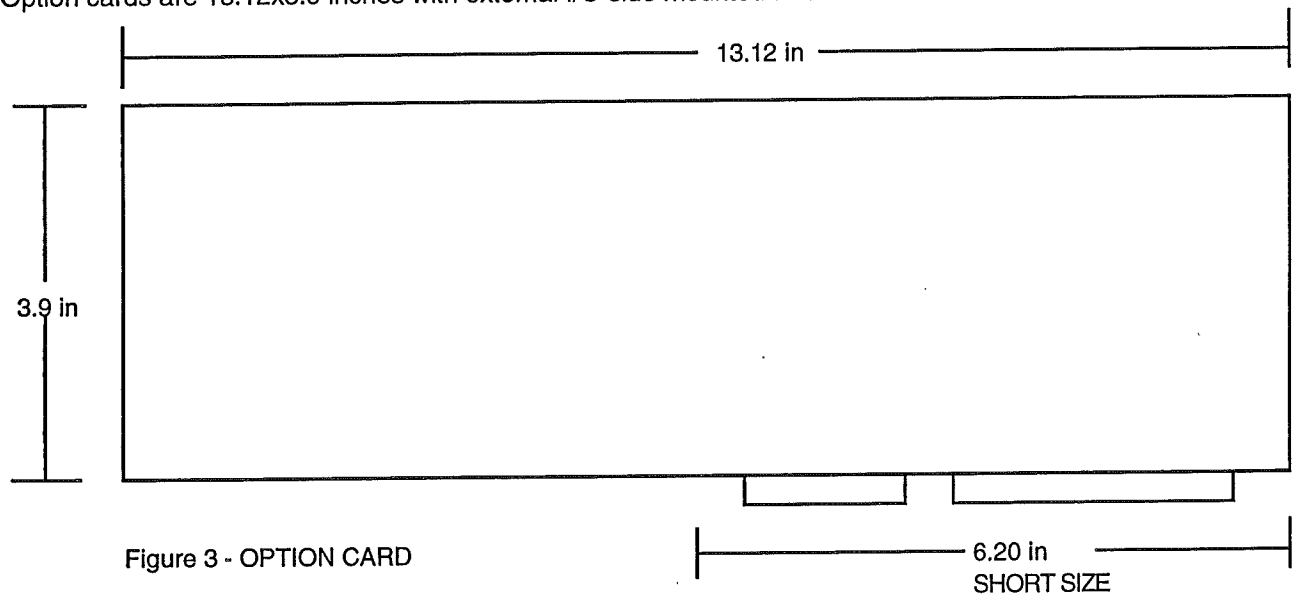


Figure 3 - OPTION CARD

2.4.1 32 Bit EXPANSION CONNECTOR

The Expantion Bus has been derived from the IBM PC AT and XT from where we get the basic card shape and pinnout. No automatic byte packing is supported. the expansion cards are for user supplied IO devices , as the main memory is in the SIMM modules on the mo ther board.

32 Data Lines
20 Address lines (4 Megabyte address range per MEMR/W and IOR/W)
3 Interrupts (IRQs)
3 Pseudo DMAs (at DRQ locations)

Option connector description (AT designation)
* = Active Low

PIN	A	B (circuit)	C	D (circuit)
1	GND (I/O CHK)	GND	BE1* (SBHE)	GND (MEM16*)
2	D07	RESET	BE2* (LA23)	GND (IO16*)
3	D06	+5V	D24 (LA22)	NC (IRQ10)
4	D05	NC (IRQ9)	D25 (LA21)	NC (IRQ11)
5	D04	NC (-5)	D26 (LA20)	DRQ4 (IRQ12)
6	D03	DRQ2	D27 (LA19)	DACK0* (IRQ15)
7	D02	NC (-12V)	D28 (LA18)	DRQ0 (IRQ14)
8	D01	NC (0 WS)	D29 (LA17)	D16 (DACK0*)
9	D00	+12V	D30 (MEMR*)	D17 (DRQ0)
10	NC (I/O CH RDY)	GND	D31 (MEMW*)	D18 (DACK5*)
11	BE0* (AEN)	MEMW*	D08	D19 (DRQ5)
12	LA21 (SA19)	MEMR*	D09	D20 (DACK6*)
13	LA20 (SA18)	IOW*	D10	D21 (DRQ6)
14	LA19 (SA17)	IOR*	D11	D22 (DACK7*)
15	LA18 (SA16)	DACK3*	D12	D23 (DRQ7)
16	LA17 (SA15)	DRQ3	D13	+5
17	LA16 (SA14)	DACK1*	D14	BE3* (MASTER*)
18	LA15 (SA13)	DRQ1	D15	GND
19	LA14 (SA12)	NC (Refresh)		
20	LA13 (SA11)	12 MHz MCLK		
21	LA12 (SA10)	NC (IRQ7)		
22	LA11 (SA09)	IRQ6		
23	LA10 (SA08)	IRQ5		
24	LA09 (SA07)	IRQ4		
25	LA08 (SA06)	IRQ3		
26	LA07 (SA05)	DACK2*		
27	LA06 (SA04)	NC (TC)		
28	LA05 (SA03)	NC (BALE)		
29	LA04 (SA02)	+5V		
30	LA03 (SA01)	NC (OSC = 7.7 Mhz)		
31	LA02 (SA00)	GND		

2.4.1.1 EXPANSION Bus line description

D0 to D7	Lowest Significant Byte of data (A0=0 A1=0)
D8 to D15	Middle Significant Byte of Data (A0=1, A1=0)
D16 to D23	Higher Significant Byte of data (A0=0, A1=1)
D24 to D31	Highest Significant Byte of Data (A0=1, A1=1)
LA2 to LA21	Latched Address 20 Bit Memory Address defines 4 MBytes of expansion addressing (32 bit word Addressable). A 4 MByte address space is defined for both memoy space (MEMR/W) and for IO space (IOR/W)
BE0*	Byte Enable 0* enables the drivers for the lowest Byte (Bits 0 to 7) on the bus.
BE1*	Byte Enable 1* enables the drivers for the middle Byte (Bits 8 to 15) on the bus.
BE2*	Byte Enable 2* enables the drivers for the upper middle Byte (Bits 16 to 23) on the bus.
BE3*	Byte Enable 3* enables the drivers for the highest Byte (Bits 24 to 31) on the bus.
MRD*	Memory Read - Active Low pulse that indicates that the bus master is reading data from memory on the bus
MWR*	Memory Write - Active low pulse that indicates that the bus master is writing to memory on the bus
IORD*	Input/ Output Read - Active Low pulse that indicates that the bus master is reading data from I/O devices on the bus.
IOWR*	Input/ Output Write - Active low pulse that indicates that the bus master is writing to I/O devices on the bus.
12CLK*	Bus Clock - 12 Mhz Clock originating from the Mo ther Board. (MCLK)
RESET	Power on reset or Bus reset both active high.
IRQ3-6	Predecoded interupt vectors / active high.hardwired to the IOC controller on the mo ther board
DRQ0-4	Pseudo DMA (Fast interupt request)
DACK*0-3	Pseudo DMA Acknowledge.
GND	Ground - there are lots of these
+5 Volts	Main Power for Boards
-5 Volts	Not Used in this version board
-12 Volts	Not Used in this version board
+12 Volts	Auxillary supplies for varied uses.

2.4.2 Logic Analyser/ WCS Connector

Pin	A	B	C	96 PIN DIN (Fem)
1	D[0]	D[1]	D[2]	
2	D[3]	D[4]	D[5]	
3	D[6]	D[7]	D[8]	
4	D[9]	D[10]	D[11]	
5	D[12]	D[13]	D[14]	
6	D[15]	D[16]	D[17]	
7	D[18]	D[19]	D[20]	
8	D[21]	D[22]	D[23]	
9	D[24]	D[25]	D[26]	
10	D[27]	D[28]	D[29]	
11	D[30]	D[31]	-	
12	MCLK	GND	FCLK	
13	MREQ	GND	TCLK	
14	NWAIT	GND	RDG	
15	NRW	+5 V	ABE	
16	NBW	+5 V	DBE	
17	ABORT	+5 V	CBE	
18	-	+5 V	MBE	
19	-	GND	NRESET	
20	ROMOE	GND	NMI	
21	DISAROM	GND	NHALT	
22	A[0]	A[1]	A[2]	
23	A[3]	A[4]	A[5]	
24	A[6]	A[7]	A[8]	
25	A[9]	A[10]	A[11]	
26	A[12]	A[13]	A[14]	
27	A[15]	A[16]	A[17]	
28	A[18]	A[19]	A[20]	
29	A[21]	A[22]	A[23]	
30	A[24]	A[25]	A[26]	
31	A[27]	A[28]	A[29]	
32	A[30]	A[31]	GND	

2.4.2.1 Logic Analyser Signal Description

Signal	Source	Destination	Description
D[0:31]	ARM CPU	System	Processor Data Bus
A[0:31]	ARM CPU	System	Processor Address Bus
FCLK	MEMC	ARM CPU	25 Mhz Processor Bus
MCLK	MEMC	ARM CPU	12.5 Mhz Memory Bus
NWAIT	MEMC	ARM CPU	Wait State Signal
NRW	ARM CPU	System	Not Read/ Write
NBW	ARM CPU	System	Not Byte/ Word
ABORT	BreakPoint	ARM CPU	Detection of Break Point Address condition
STRB1	BreakPoint	Logic Analyser	Strobe for Logic Analyser (N/ C in this Board)
STRB2	BreakPoint	Logic Analyser	Strobe for Logic Analyser (N/ C in this Board)
ROMOE	MEMC	ROM	ROM output enable- used for (WCS)
MREQ	ARM CPU	MEMC	Mem ory Request Snignal
TCLK	PAL22V10	Logic Analyser	Test Clock to Partner ET ROM ICE
CPCLK	PAL22V10	Logic Analyser	Read Gate Strobe to Partner ET ROM ICE
ABE	BreakPoint	ARM CPU	Address Bus Enable
DBE	BreakPoint	ARM CPU	Data Bus Enable
CMBE	BreakPoint	ARM CPU	Control Bus Enable
NRESET	Reset Logic	System	Negative Reset Signal
NMI	BreakPoint	INTC	Non Maskable FIQ input
HALT	BreakPoint	MEMC	Force nWAIT Condition

2.4.3 Modular CPU Connector

Pin	A	B	C	96 PIN DIN (Fem)
1	GND	D[0]	D[1]	
2	D[2]	D[3]	D[4]	
3	D[5]	D[6]	D[7]	
4	D[8]	D[9]	GND	
5	D[10]	D[11]	D[12]	
6	VCC	D[13]	D[14]	
7	D[15]	D[16]	D[17]	
8	D[18]	GND	D[19]	
9	D[20]	D[21]	D[22]	
10	D[23]	D[24]	D[25]	
11	D[26]	D[27]	D[28]	
12	D[29]	D[30]	D[31]	
13	DBE	TCK	nMREQ	
14	GND	nIRQ	GND	
15	nFIQ	ABORT/nPREQ	nTRST	
16	VCC	nRESET	TMS	
17	A[30]/nPFIQ	/nPIRQ	FCLK/RCLK	
18	ABE	GND	nRW	
19	nBW	LOCK	TDO	
20	nWAIT	TDI	MCLK	
21	A[0]	A[1]	A[2]	
22	A[3]	A[4]	A[5]	
23	A[6]	A[7]	A[8]	
24	A[9]	A[10]	GND	
25	A[11]	A[12]	A[13]	
26	VCC	A[14]	A[15]	
27	A[16]	A[17]	A[18]	
28	A[19]	GND	A[20]	
29	A[21]	A[22]	A[23]	
30	A[24]	A[25]	A[26]	
31	A[27]	A[28]	A[29]	
32	GND	/A[31]	GND	

/ signals protected by jumpers on the CPU Module
These signal are not used or are used differently on the Acorn 486 CPU module

2.4.3.1 Modular CPU Signal Description

Signal	Source	Destination	Description
D[31:0]	ARM CPU	System	Bidirectional Data Bus
A[31:0]	ARM CPU	System	Processor Address Bus
FCLK	MEMC	ARM CPU	25 Mhz Processor Bus
MCLK	MEMC	ARM CPU	12.5 Mhz Memory Bus
NWAIT	MEMC	ARM CPU	Wait State Signal
NRW	ARM CPU	System	Not Read/ Write
NBW	ARM CPU	System	Not Byte/ Word
ROMOE	MEMC	ROM	ROM output enable- used for (WCS)
MREQ	ARM CPU	MEMC	Mem ory Request Snignal
NOPC	ARM CPU	Logic Analyser	Opcode Request - Istruction on CPD bus
CPCLK	ARM CPU	Logic Analyser	Co-Processor Clock
ABE	BreakPoint	ARM CPU	Address Bus Enable
DBE	BreakPoint	ARM CPU	Data Bus Enable
CMBE	BreakPoint	ARM CPU	Control Bus Enable
NRESET	Reset Logic	System	Negative Reset Signal
NMI	BreakPoint	INTC	Non Maskable FIQ input
HALT	BreakPoint	MEMC	Force nWAIT Condition

2.3.4 Serial Port

A Serial Port is provided for communication to the host or for applications.

Serial Port 1 D-Subminiature PIN	Serial Port 2 HEADER PIN		DESCRIPTION
1	1		
2	3	IN	Receive Data
3	5	OUT	Transmitter Data
4	7		
5	9		GND
6	2		
7	4	OUT	RTS - Ready to Send output
8	6	IN	CTS- Clear to Send input
9	8		
	10		NU

Note: Dual Row Header is not used on the VY86PID

2.3.5 10Base-T Ethernet

An Ethernet 10Base-T RJ-45 connector is provided for fast communication to the host or for applications.

RJ-45	NAME	DIR	DESCRIPTION
1	TPP	OUT	Transmitter Data
2	TPN	OUT	Transmitter Data
3	RPP	IN	Receive Data
4			
5			
6	RPN	IN	Receive Data
7			
8			

2.3.6 Parallel Port

The Parallel port is used primarily for control of a Line or Page Printer . Because the parallel port is bi-directional it can be used for input as well as output. Several plugin peripherals, such as E thernet adapters , have now taken advantage of this useful interface.

D-SHELL PIN	HEADER PIN	DESCRIPTION	
1	1	O	-STROBE
2	3	I/O	Data0
3	5	I/O	Data1
4	7	I/O	Data2
5	9	I/O	Data3
6	11	I/O	Data4
7	13	I/O	Data5
8	15	I/O	Data6
9	17	I/O	Data7
10	19	I	-ACK
11	21	I	BUSY
12	23	I	PE
13	25	I	SLCT
14	2	O	-AUTOFEED XT
15	4	I	-ERROR
16	6	O	-INIT
17	8	O	-SLCTIN
18	10	GND	
19	12	GND	
20	14	GND	
21	16	GND	
22	18	GND	
23	20	GND	
24	22	GND	
25	24	GND	
	26	N.U.	

Note: Dual Row Header is used on the PID3.

3.0 SYSTEM MEMORY SPACE ALLOCATION

3.1 MEMORY MAP

000 0000 to 0FF FFFF	DRAM - 1 to 16 MBytes. One Bank of DRAM in 4 SIMMs 8 256Kx4 = 1 MByte 4 512Kx8 = 2 Mbyte 8 1MBx4 = 4 MByte 32 4Mbx1 = 16 Mbyte DRAM is repeated within the 16 MByte space After Reset ROM is located here.
100 0000 to 1FF FFFF	DRAM - Bank 2 (not used on this board.)
200 0000 to 2FF FFFF	I/O control is mapped to this space - 16 Mbytes Used for both internal and external peripherals
300 00 00 to 3FF FFFF	ROM, EPROM, or Writable control store

3.1.1 Software Vectors

ADDRESS VECTOR	INSTRUCTION DESCRIPTION	
000 0000 Reset vector	LDR PC,[PC, #Vector offset]	Load Soft Vector to ROM Reset
000 0004 Undef Inst	LDR PC,[PC, #Vector offset]	Load Soft Vector to ROM FP Emulator
000 0008 Software Int	LDR PC,[PC, #Vector offset]	Load Soft Vector to SWI Dispatcher
000 000C Abort Inst	LDR PC,[PC, #Vector offset]	Load Soft Vector to ROM routine
000 0010 Abort Data	LDR PC,[PC, #Vector offset]	Load Soft Vector to ROM routine
000 0014 reserved		
000 0018 Normal Int	LDR PC,[PC, #Vector offset]	Load Soft Vector to IRQ dispatcher
000 001C Fast Int	LDR PC,[PC, #Vector offset]	Load Soft Vector to FIRQ dispatcher

3.2 I/O Memory Map 200 0000 to 2FF FFFF General I/O area divided as below:

200 0000 to 23F FFFF Internal Functions

240 0000 to 240 001C Expansion Slot Pseudo DMA (needs PAL)

REG	Name	R/W	Description
0000	DACK0	R/W	IOR/W asserted with DACK0
0004	DACK1	R/W	IOR/W asserted with DACK2
0008	DACK2	R/W	IOR/W asserted with DACK3
000C	DACK3	R/W	IOR/W asserted with DACK3
0010	DACK0 TC	R/W	IOR/W asserted with DACK0 and TC
0014	DACK1 TC	R/W	IOR/W asserted with DACK1 and TC
0018	DACK2 TC	R/W	IOR/W asserted with DACK2 and TC
001C	DACK3TC	R/W	IOR/W asserted with DACK3 and TC

280 0000 to 2BF FFFF Expansion Slot I/O Space (-IOR, -IOW generated)

2C0 0000 to 2FF FFFF Expansion Slot Memory Space (-MRD, -MWR generated)

3.3 200 0000 to 204 FFFF Internal Functions

3.3.1 INTWT PGA addressed from 200 0000 to 200 000C

0000	IRQS	R	IRQ Status
0000	IRQRST	W	IRQ RESET
0004	IRQM	W	IRQ MASK
0008	FIQS	R	FIQ Status
000C	FIQM	W	FIQ MASK
0010	FIQto IRQ	W	FIQ to IRQ bit
0010	Timer Low	R	low bits of timer + FIQtoIRQ bit
0018	Latch_Time	W	Latch time instantaneous value
0018	Timer High	W	high bit of timer

3.4 200 0020 to 200 003C 16C552 Serial port1
200 0040 to 200 004C 16C552 Serial port2

REG	Name	R/W	Description
0020	RBR/THR	R-W	Receive Buffer Register - Transmitter Holding Register
0024	IER	R/W	Interupt Enable Register (Bidirectional)
0028	IIR	R	Interupt Identification (read only)
002C	LCR	R/W	Line Control Register
0030	MCR	R/W	Modem Control Register
0034	LSR	R	Line Status Register
0038	MSR	R	Modem Status Register
003C	SR	R/W	Scratch Register
0020	(DLAB)	R/W	Divisor Latch LSB
0024	(DLAB)	R/W	Divisor Latch MSB

3.5 200 0060 to 200 006C 16C552 Parallel Port

REG	Name	R/W	Description
0060	PDOUT	R/W	Data Output/Input Register
0064	PSTAT	R	Printer Status Register
0068	PCON	R/W	Printer Control Register
006C	GPIO	R/W	General Porpose Input/ Output Pins

3.6 204 0020 to 204 003C E thernet (SMC91C94)

REG	Bank0	Bank1	Bank2	Bank3
0020	TCR	CONFIG	MMU	MT0
0024	EPH	BASE	PNR/ARR	MT3
0028	RCR	IA0	FIFO	MT4
002C	COUNT	IA2	POINTER	MT6
0030	MIR	IA4	DATA	-
0034	MCR	GENERAL	DATA	-
0038	RESV	CONTROL	INTERRUPT	-
003C	BANK	Select register bank - common to all banks		

Note: Descriptions in E thernet section

3.7 240 0020 LED Port (write only)

Writing a zero in any bit position will light the corresponding LED.

4.0 Input/ Output Register Description

4.1 INTC PGA 200 00 00 to 200 001C

The INTWT (Interrupt with Timer) Programmable Gate array provides for low level control of 9 IRQ sources and 8 FIQ sources. All register are ei ther read only or write only. Thus the software needs to keep a shadow of the IRQ and FIG masks.

REG	Name	R/W	Description
0000	IRQS	R	IRQ Status
0000	IRQRST	W	IRQ RESET
0004	IRQM	W	IRQ MASK
0008	FIQS	R	FIQ Status
000C	FIQM	W	FIQ MASK
0010	FIQto IRQ	W	FIQ to IRQ bit
0010	Timer Low	R	low bits of timer + FIQtoIRQ bit
0018	Latch_Time	W	Latch time instantaneous value
0018	Timer High	W	high bit of timer

4.1.1 IRQS IRQ Status Register (address 200 0000)

This Register containes the interrupt input with masking. A bit in this register is anded with the coresponding mask bit in the IRQM register and then "ored" with all the o ther bits to generate the IRQ.

REG	7	6	5	4	3	2	1	0
IRQS	PANIC	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0

Bit 7	PANIC	This bit is set when the panic button input is pulsed low This bit is reset by writing reset location.
Bit 6	IRQ6	Connected to Expansion Slot IRQ6
Bit 5	IRQ5	Connected to Expansion Slot IRQ5
Bit 4	IRQ4	Connected to Expansion Slot IRQ4
Bit 3	IRQ3	E thernet Interrupt
Bit 2	IRQ2	Parallel Port Interrupt
Bit 1	IRQ1	Timer (approximately 10 Milli-second periodic interupt)
Bit 0	IRQ0	Serial Port 1

4.1.2 IRQRST IRQ Reset Port (address 200 0000)

Bit 7 Writing this bit set to 1 will reset thePANIC interrupt bit.
Bit 1 Writing this bit set to 1 will reset the timer interrupt bit.

4.1.3 IRQM IRQ Mask Register (address 200 0004)

Writing a "one" to bits 6-0 will enable the corresponding interrupt bit. This register is reset on power on.

REG	7	6	5	4	3	2	1	0
IRQM	ON	ENIRQ6	ENIRQ5	ENIRQ4	ENIRQ3	ENIRQ2	ENIRQ1	ENIRQ0

* note Panic is always enabled

4.1.4 FIQS FIQ Status Register (address 200 0008)

This Register containes the raw fast interrupt input (without masking). A bit in this register is anded with the corresponding mask bit in the FIQM register and then "ored" with all the o ther bits to generate the FIQ

REG	7	6	5	4	3	2	1	0
FIQS	DRQ3	DRQ2	DRQ1	DRQ0	NMI	IRQ7	RXRQ1	TXRQ1

Bits 7-4	DRQ3-0	Expansion Slot DMA Request
Bit 3	NMI	Logic Anaylser Port
Bit 2	IRQ7	Serial Port Interrupt
Bit 1	RXRQ1	Serial Port 1 Receive DMA Request
Bit 0	TXRQ1	Serial Port 1 Transmit DMA Request

4.1.3 FIQM FIQ Mask Register (address 200 000C)

Writing a "one" to bits 7-0 will enable the corresponding interrupt bit. This register is reset on power on.

4.1.4 TimerLow - Latched Timer plus FIQ_to_IRQ bit (address 200 0010)

Read only - the counting resolution of the timer is 4 MCLKS or 320 ns. Bit 0 revels the state of the FIQ_to_IRQ bit, used in Helios and o ther RTOSes.

REG	7	6	5	4	3	2	1	0
TimerLow	T[7]	T[6]	T[5]	T[4]	T[3]	T[2]	T[1]	FIQ_to_IRQ

4.1.5 TimerHigh - Latched Timer (address 200 0018)

Read only

REG	7	6	5	4	3	2	1	0
TimerLow	T[15]	T[14]	T[13]	T[12]	T[11]	T[10]	T[9]	T[8]

4.1.6 FIQ_to_IRQ - Write FIQ_to_IRQ bit (address 200 0010)

Write only register used for the FIQ_to_IRQ bit.

REG	7-1	0
FIQ_to_IRQ	Don't Care	FIQ_to_IRQ

Writing the FIQ_to_IRQ will set the IRQ to the processor. This provides a method for the FIQ handler to signal to the IRQ hander for operating system uses.

4.1.7 LatchTimer- (address 200 0018)

Write to latch current time into the time latch where it can be read by the processor the Output Data is ignored. Writing the LatchTimer will store the current time synchonously to the timer latch. O therwise the timer operation would be asynchronous and very difficult to use.

5.0 16C551 Serial Port Registers [200 0020 to 200 006C]

The 16C551 2 - 8252 UARTs (wuth FIFOs), and an 8 bit parallel bidirectional centronics printer interface

5.1 Serial Interfaces (200 0020 to 200 005C)

The 16C552 has two 16C550 cells with 16 byte data FIFOs for maximum performance in data transfers from the host computer. the UARTs are described in detail below. For more information, see the VLSI Technology VL16C552 datasheet.

The regsters associated with the UARTs are as follows:

REG	Ser1	Ser2	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
RBR	0020	0040	R/O	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
THR	0020	0040	W/O	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
IER	0024	0044	R/W	-	-	-	-	EDSSI	ELSI	ETBEI	ERBFI
IIR	0028	0048	R/O	IIR7	IIR6	-	-	FIFEN	IID1	IID0	IPENDN
FCR	0028	0048	W/O	FTL1	FTL0	-	-	RMODE	TFCLR	RFCLR	FIFOEN
LCR	002C	004C	R/W	DLAB	BREAK	STICK	EVPAR	PAREN	SBSEL	WLS1	WLS0
MCR	0030	0050	R/W	-	-	-	LBACK	-	-	RTS	DTR
LSR	0034	0054	R/W	ERFIFO	TEMT	THRE	ERBRK	ERFRM	ERPAR	EROVR	RDR
MSR	0038	0058	R/W	-	-	DSR	-	-	-	DDSR	-
SCR	003C	005C	R/W	D7	D6	D5	D4	D3	D2	D1	D0
DLL	0020	0040	W-O	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
DLM	0024	0044	W-O	DL15	DL14	DL13	DL12	DL11	DL10	DL9	DL8

5.1.1 Serial Port Data Registers (RBR, THR) (Address 200 0020/40)

Received data at the SRXD input pin is shifted into the Receiver Shift Register by the 16X clock provided from the baud rate generator. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Data Register (RBR). the Read Data Ready (RDR) flag in the Serial Port Status Register (LSR) is set.

FIFO (and double) buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the overflow of the data in the register. the Overrun Error (EROVO) flag in the LSR register indicates the overrun condition.

During Transmit operation, the Transmitter Holding Register holds parallel data from the internal data bus until the Transmitter Shift Register is empty and ready to accept a new character. Data Bit 0 is the first bit transmitted. the Transmit Holding register Empty (THRE) flag in LSR reflects the current status.

The contents of the Receive Buffer Register follows below :

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
RBR	0000	R/O	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

The contents of the Transmit Holding Register follows below:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
THR	0x030	W/O	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

5.1.2 Interrupt Enable Register (IER) (Address 200 0024/44)

The Interrupt Enable Register is used to independently enable the four types of serial channel interrupts.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
IER	0x031	R/O	-	-	-	-	EDSSI	ELSI	ETBEI	ERBFI

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
0	ERBFI	R/O	0	Enable Received Data Available Interrupt [and Timeout Interrupt in FIFO mode for Host UART only]
1	ETBEI	R/O	0	Enable Transmitter Holding Reg Empty Interrupt
2	ELSI	R/O	0	Enable Receiver Line Status Interrupt
3	EDSSI	R/O	0	Enable Modem Status Interrupt
7:4	RESV	-	-	Not Used

5.1.3 Interrupt Identification Register (IIR) (Address 200 0028/48)

The Interrupt Identification Register is a read only register used to identify the four types of serial channel interrupts.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
IIR	0028	R/O	IIR7	IIR6	-	-	FIFEN	IID1	IID0	IPENDN

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
0	IPENDN		R/O	Set to 0 if ANY Interrupt is pending.
2:1	IID[1:0]	R/O	0	Interrupt Type bits [1:0] (see table below).
3	FIFEN	R/O	0	0=16C450 Mode, 1=16C550 Mode (FIFO enabled).
5:4	RESV	-	-	Not Used - Always 0.
7:6	IIR[7:6]	R/O	0	FCR[0]=1 sets these two bits.

IIR Table of Pending Interrupts

Int ID Bits		Priority		
3 2 1 0	Level	Int Flag	Int Source	Int Reset Control
X X X 1		None		None
0 1 1 0	First	Recvr Line Status	OE, PE, FE, or BI	LSR Read
0 1 0 0	Second	Recvd Data Avail		RBR Read
1 1 0 0*	Second	FIFO Status, FIFO thresh and wait timeout		RBR Read
0 0 1 0	Third	THRE		IIR Read if THRE is the source, else THR Write
0 0 0 0	Fourth	Modem Status	-CTS, -DSR, -RI, -RSLD	MSR Read

5.1.4 FIFO Control Register (FCR) (Address 200 0028/48)

The FIFO Control Register Register is used to control the operation of the built-in data FIFOs. This register is write only.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
FCR	0028	W/O	FTL1	FTL0	-	-	RMODE	TFCLR	RFCLR	FIFOEN

Bit	Name	R/W	Reset	Use
0	FIFOEN		W/O	0 When set to 1, enables both receive and transmit FIFOs.
1	RFCLR	W/O	0	Writing a 1 to this bit clears the Receive FIFO.
2	TFCLR	W/O	0	Writing a 1 to this bit clears the Transmit FIFO.
3	RMODE		W/O	0 Changes the RXRDY and TXRDY pins from mode 0 to mode 1
5:4	RESV	-	-	Not Used.
7:6	FTL[1:0]		W/O	00? Receive FIFO trigger level:

FTL1	FTL0	Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

5.1.5 Line Control Registers (LCR) (Address 200 002C/4C)

The format of the characters transmitted and received are controlled by the Line Control Registers.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
LCR	002C	R/W	DLAB	BREAK	STICK	EVPAR	PAREN	SBSEL	WLS1	WLS0

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
1:0	WLS[1:0]		R/W	0

Word Length Select:

WLS1	WLS0	Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

2 SBSEL R/W 0 Stop Bit Select. This bit specifies the number of stop bits in each transmitted character. When set to 0, one stop bit is generated. When set to 1, 1.5 stop bits stop bits are generated if 5 data bits are selected, but 2 stop bits are generated if 6, 7, or 8 data bits are selected. the receiver checks for the appropriate number of stop bits.

3 PAREN R/W 0 Parity Enable. When set to 1, a parity bit is generated and checked.

4 EVPAR R/W 0 Parity Select. When parity is enabled, this bit selects odd parity (0) or even parity (1).

5 STICK R/W 0 Stick Parity. When parity is enabled, a 1 causes transmission and reception of a parity bit to be in the opposite state from that indicated by EVPAR. This allows forced parity to a known state.

6 BREAK R/W 0 Force Break. When set to 1, the serial output (TXD) is forced to the spacing (0) state. the break is disabled by setting this bit to 0.

the width of the break pulse created is a function of software. As a result, the first character transmitted following a break condition might have a framing error, and should be discarded. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break: after THRE load THR with all "0"'s, set BREAK bit in responce to the next THRE. Wait for TEMT=1, then reset BREAK when normal transmission has to be restored..

7 DLAB R/W 0 Divisor Latch Bit. When set, addresses 020 and 024) access the UART clock divider latches.

5.1.6 MODEM Control Register (MCR) (Address 200 0030/50)

The DTR pin and loop back function are controlled by the Modem Control Registers:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
HMCR	0030	R/W	-	-	-	LBACK	-	-	RTS	DTR

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
0	DTR	R/W	0	Data Transmitter Ready. When set to 1, the DTR output pin is forced low.
1	RTS	R/W	0	Request to Send. When set to 1, the RTS output is forced low.
3:2	RESV	-	-	Reserved.
4	LBACK	R/W	0	Loopback Enable. This bit provides a local loopback feature for diagnostic testing of the serial channel. When set to 1, the Transmit Data output pin (TXD) is set to the marking state (1), and the Receive Data input pin (RXD) is disconnected. the output of the Transmitter is looped back into the Receiver. the handshake input pin (DSR) is disconnected. the handshake output pins (DTR) are held in their inactive state (1). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the serial channels.
7:5	RESV	-	-	Reserved.

5.1.7 Line Status Registers (LSR) (Address 200 0034/54)

The Line Status Registers hold the current status of the UART:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
HLSR	0034	R/W	ERFIFO	TEMT	THRE	ERBRK	ERFRM	ERPAR	EROVR	RDR

Error flags ERBRK, ERFRM, ERPAR, ERFIFO, and EROVR provide the status of any error conditions detected in the receiver. During reception of the stop bit(s), the error flags are set by an error condition. the error flags are not reset by the absence of an error condition in the next received character. the flags reflect the last character only if no overrun occurred.

In the LSR the setting of status bits is inhibited during status register read operations by the CPU. If a status condition is generated during a read operation, the status bit is not set until the trailing edge of the read.

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use	
0	RDR	R/W	0		Receive Data Ready. This bit indicates that the Receiver Buffer Register has been loaded with a received character (including Break) and that the CPU may access this data. Reset whenever register is read.
1	EROVR	R/W	0		Receive Overrun Error. This bit indicates that the character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. the first character is thereby lost. Reset whenever register is read.
2	ERPAR	R/W	0		Parity Error. This bit is set when the last character received has a parity error based on the programmed versus calculated parity. Reset whenever register is read.
3	ERFRM	R/W	0		Framing Error. This bit indicates that the last character received contained an incorrect number of stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Reset whenever register is read.
4	ERBRK	R/W	0		Break Detect Error. This bit indicates that the last character received was a break character, i.e. the received data input was held low (0) for longer than a full word transmission time (start bit + data bits + parity + stop bits). Reset whenever register is read.
5	THRE	R/W	1		Transmitter Holding Register Empty. This bit indicates that the THR register is empty and may receive another character. Reset whenever THR is written to.
6	TEMT	R/W	1		Transmitter Empty. This bit is set to 1 when the Transmitter Holding Register THR and the Transmitter Shift Register are both empty. It is reset whenever HTHR/VTHR is written to, and remains low until the character is transferred out of the TXD pin.
7	ERFIFO	R/W	0		FIFO Error . This bit is set to 1 if the receiver FIFO is full and another

character is received.

5.1.8 MODEM Status Register (MSR) (Address 200 0038/58)

The Modem Status Register holds the current status of the SDSR/VUDSR pin:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
MSR	0038	R/W	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
0	DCTS	R-O	-	Delta Clear to Send
1	DDSR	R-O	-	Delta DSR. This bit indicates that the DSR pin has changed state since the last time it was read. Not used on this board.
2	TERI	R-O	-	Trailing Edge Ring Indicator. Not used on this board.
3	DDCD	R-O	-	Delta Data Set Ready. Not used on this board.
4	CTS	R-O	-	Clear To Send. Reflects status of CTS pin on Serial Interface
5	DSR	R-O	-	Data Set Ready. This bit always reflects the value of the DSR pin . Not used on this board.
6	RI	R-O	-	Ring Indicator . Not used on this board.
7	DCD	R-O	-	Data Carrier Detect . Not used on this board.

5.1.9 Scratch Registers (SCR) (Address 200 003C/5C)

The Scratch Register holds the a read/write byte that affects no operations in the UART:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
SCR	003C	R/W	D7	D6	D5	D4	D3	D2	D1	D0

5.1.10 Divisor Latch Registers (DLL and DLM) (Address 200 0020/40 and 0024/44)

These registers control the Baud Rate Generator divisor, and are only accessible when bit 7 (DLAB) in the LCR registers are set.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
DLL	0020	R/W**	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
DLM	0024	R/W**	DL15	DL14	DL13	DL12	DL11	DL10	DL9	DL8

**accessible only when LCR[7]=1.

The baud rate generator can use a 1.8432, 2.4576, or 3.072 MHz input clock. This clock is input on the SCLK pin and is used by both the Host and Video UARTs. With these frequencies, standard bit rates from 50 to 38.5K bps are available. Divisors for some popular baud rates are shown below:

Baud Rate	1.8432 MHz	2.4576 MHz	3.072 MHz
1200	96	128	160
2400	48	64	80
9600	12	16	20
19200	6	8	10
38400	3	4	5

5.2 Parallel Interface (200 0060 to 200 007C)

5.2.1 Register Overview

The following registers are contained in the Parallel Port logic:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
PDRW	0060	W/R	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PSR	0064	R/O	-BSY	-ACK		PE	SLCT	-ERR		1 1 1
PCR	0068	W/R	1	1	DIR	ENIRQ	SLIN	-INIT	AFD	STB

5.2.2 Parallel Data Read and Write Registers (PDRW) (Address 200 0060)

A single address is used for these two registers - one for reads and one for writes. A read from PDR reflects the current state of the Printer Data Port (PRD[7:0]) pins, while a write to PDW sets the state of the Printer Data Port pins.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
PDR	0060	R/O	PDI7	PDI6	PDI5	PDI4	PDI3	PDI2	PDI1	PDI0
PDW	0060	W/O	PDO7	PDO6	PDO5	PDO4	PDO3	PDO2	PDO1	PDO0

The detailed bit definition of the PDR is as follows:

Bit	Name	R/W	Reset	Use
0	PDI0	R/O	0	Printer Data Port Input bit 0
				. . .
7	PDI7	R/O	0	Printer Data Port Input bit 7

The PDW register is normally used in data transfers to external devices. the detailed bit definition of the PDW is as follows:

Bit	Name	R/W	Reset	Use
0	PDO0	W/O	0	Printer Data Port Output bit 0
				. . .
7	PDO7	W/O	0	Printer Data Port Output bit 7

5.2.3 Parallel Status Register (PSR) (Address 200 0064)

This register senses the status of the handshake signals from the host computer:

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
PSR	0064	R/O	-BSY	-ACK	PE	SLCT	-ERR	1	1	1

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
0-2	resv	R		Always read as 1
3	-ERR	R		Staust of ERR pin
4	SLCT	R		Status of SLCT pin
5	PE	R		Status of PE pin
6	-ACK	R		Status of ACK pin
7	-BSY	R		Status of BSY pin

5.2.4 Parallel Control Register (PCR) (Address 200 0064)

This register controls printer status that is returned to the host computer.

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
PCR	0068	R/W	1	1	DIR	ENIRQ	SLIN	-INIT	AFD	STB

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
0	-STB	R/W	0	Data Strobe, 1=STB pin low
1	-AFD	R/W	0	Auto Feed, 1=AFD pin low
2	INIT	R/W	0	Initialise Printer, 1=INIT pin high
3	SLIN	R/W	0	Select In, 1=SLIN pin high
4	ENIRQ	R/W	0	Enable Interrupt, 1=Enable interrupt from the ACK signal asserted low
5	DIR	R/W	0	Direction, 1=Ouput buffers are disabled allowing PD bus to be input.
6-7	resv			

5.3 E thernet Interface (204 0020 to 204 003C)

PID3 uses the SMC91C92 to provide E thernet communications for fast download and support of TCP/IP services for embedded operating systems. the advantqages of this part are low cost, internal RAM, and straight forward programming. Since the SMC91C92 was designed for residence on the ISA bus, it conserves scarce ISA IO space by folding its 22 16 bit registers into 4 banks of 16 registers. Bank switching is achieved through the use of the Bank Switch register which is accessable at location 5C in all banks.

REG	Bank0	Bank1	Bank2	Bank3
0020	TCR	CONFIG	MMU	MT0
0024	EPH	BASE	PNR/ARR	MT3
0028	RCR	IA0	FIFO	MT4
002C	COUNT	IA2	POINTER	MT6
0030	MIR	IA4	DATA	-
0034	MCR	GENERAL	DATA	-
0038	RESV	CONTROL	INTERRUPT	-
003C	BANK	Select register bank - common to all banks		

5.3.1 Bank Register (Address 200 005C - All Banks)

The bits of the Bank Register are defined as follows:

REG	ADDR	TYPE	D15	D14	D13	D12	D11	D10	D9	D8
BANK	005C	R/W	0	0	1	1	0	0	1	1

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
BANK	005C	R/W	X	X	X	X	X	X	BNK1	BNK0

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
15:8	flag	R	33	Indicates that a valid 91C92 has been found
7:2	resv	R	??	Don't Care bits
1:0	BNK	R/W	00	Bank Number 0,1,2,3

5.3.2 Transmit Control Register TCR (Address 200 0040 - Bank 0)

The bits of the TCRr are defined as follows:

REG	ADDR	TYPE	D15	D14	D13	D12	D11	D10	D9	D8
TCR	0040	R/W	X	X	INLP	SSQT	FDUP	MON	X	NOCRC

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
TCR	0040	R/W	PADEN	X	X	X	X	FCOL	LOOP	TXENA

The detailed bit definition is as follows:

Bit	Name	R/W	Reset	Use
15:14	resv		??	
13	INLP	R/W	0	Internal Loop - NRZ only, does not exercise the encoder/decoder blocks
12	SSQT	R/W	0	Stop Transmission on SQET error (Signal Quality Error Test)
11	FDUP	R/W	0	Full Duplex operation. Reciever will receive frames even which transmitting.
10	MON	R/W	0	Monitor Carrier. If set the trasnsmitter will stop if it doesn't detect its one carrier.
9	resv			
8	NOCRC	R/W	0	No CRC will be apended to the transmit fram if this bit is set.
7	PADEN	R/W	0	When set the SMC91C92 will extend short frames to 64 bytes with zero's.
6:3	resv			
2	FCOL		0	Force Collision. When set the transmitter will force a collision. This bit is then reset.
1	LOOP	R/W	0	THis bit will cause the transmit data to be looped back to the receiver after the encoder and back through the decoder. Collision and carier sense are ignored.
0	TXENA	R/W	0	Transmit Enable. Transmit enabled when set, disabled when clear. If this bit is cleared the current frame will complete. If an error condition causes the transmitter to stop this bit will be cleared.

LOOP BACK MODES

AUI	INLP	LOOP	FDUP	LOOPS AT	TRANSMITS TO NET
X	1	X	X	NRZ MAC	N
X	0	1	1	ENDEC	N
1	0	0	1	Cable	Y
0	0	0	1	10Base-T driver	Y